Appendix 3

MC6847 data sheet

Supplied courtesy of Motorola Semiconductors.

The information here has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Motorola reserves the right to make changes to any products herein to improve reliability, function or design. Motorola does not assume any liability arising out of the application or use of any product or circuit described herein. No licence is conveyed under patent rights in any form. When this document contains information on a new product, specifications herein are subject to change without notice.

MOTOROLA Semiconductors

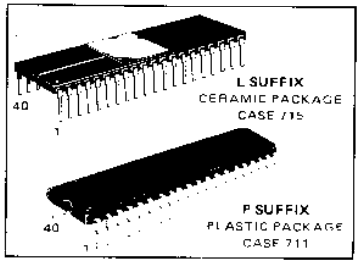
Colvilles Road, Kelvin Estate - East Kilbride/Glasgow - SCOTLAND

MC6847
NONINTERLACE
MC6847Y
INTERLACE

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

VIDEO DISPLAY GENERATOR



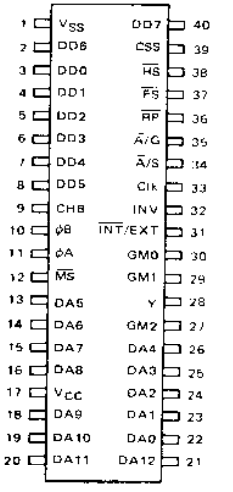
VIDEO DISPLAY GENERATOR (VDG)

The Motorola MC6847 Video Display Generator (VDG) provides a means of interfacing the Motorola M6800 microprocessor family (or similar products) to a commercially available color or black and white television receiver. Applications of the VDG include video games, bioengineering displays, education, communications and any place graphics are required.

The VDG reads data from memory and produces a composite video signal which will allow the generation of alphanumeric or graphic displays. The generated composite video may be up modulated to either Channel 3 or 4 by using the compatible MC1372 (TV Chroma and Video modulator). The up modulated signal is suitable for application to the antenna of a color TV. A typical TV game is indicated in Figure 1.

- Generates four different alphanumeric display modes and eight graphic display modes
- Compatible with the M6800 family
- Compatible with the MC1372 modulator
- The alphanumeric modes display 32 characters per line by 16 lines
- An internal multiplexer allows the use of either the internal ROM or an external character generator
- An external character generator can be used to extend the internal character set for "limited graphic" shapes
- A Mask Programmable internal character generator ROM is available on special order (Appendix A)
- One display mode offers 8-color 64 x 32 density graphics in an alphanumeric display mode
- One display mode offers 4-color 64 x 48 density graphics in an alphanumeric display mode
- All alphanumeric modes have a selectable video inverse
- Generates full video signal
- Generates R-Y and B-Y signals for external color modulator
- Full-graphic modes offer 64 x 64, 128 x 64, 128 x 96, 128 x 192, or 256 x 192 densities
- Full-graphic modes allow 2-color or 4-color data structures
- Full-graphic modes use one of two 4-color sets or one of two 2-color sets
- Available in either an interlace mode (NTSC Standard) or a non-interlace mode

PIN ASSIGNMENT

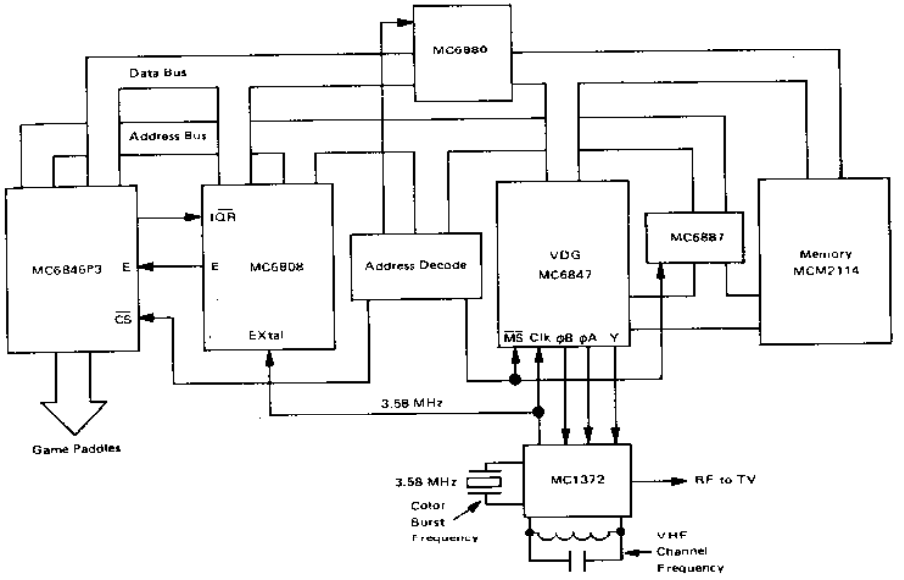


This is advance information and specifications are subject to change without notice.

Reprint

AD: 492 R2

FIGURE 1 – BLOCK DIAGRAM OF USE OF THE VDG IN A TV GAME



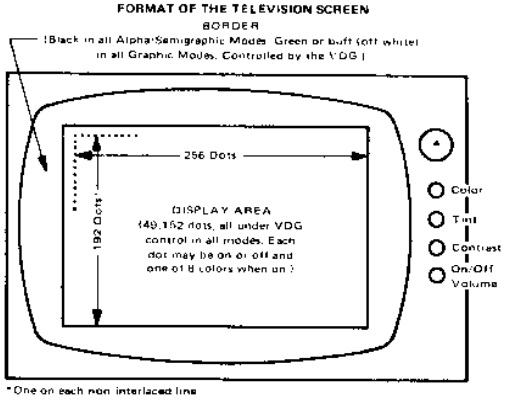
Mnemonic	Pin Numbers	Function
V_{CC}	17	+5V
V_{SS}	1	Ground
CLK	33	Color burst clock 3.579545 MHz (input)
DA0-DA12	22, 23, 24, 25, 26 13, 14, 15, 16, 18, 19, 20, 21	Address lines to display memory, high impedance during memory select ($\overline{MS}$)
DD0-DD5	3, 4, 5, 6, 7, 8	Data from display memory RAM or ROM
DD6, DD7	2, 40	Data from display memory in graphic mode; data also in alpha external mode; color data in alpha semigraphic 4 or 6
φA, φB, Y	11, 10, 28	Chrominance and luminance analog (R-Y, B-Y, Y) output to RF modulator (MC1372)
CHB	9	Chroma bias; reference φA and φB levels
$\overline{RP}$	36	Row preset – Output to provide timing for external character generator.
$\overline{HS}$	38	Horizontal Sync – Output to provide timing for external character generator.
INV	32	Inverts video in all alpha modes
$\overline{INT}$/EXT	31	Switches to external ROM in alpha mode and between SEMIG-4 and SEMIG-6 in semigraphics
$\overline{A}/S$	34	Alpha/Semigraphics; selects between alpha and semigraphics in alpha mode
$\overline{MS}$	12	Memory select forces VDG address buffers to high-impedance state
$\overline{A}/G$	35	Switches between alpha and graphic modes
$\overline{FS}$	37	Field Synchronization goes low at bottom of active display area.
CSS	39	Color set select; selects between two alpha display colors or between two color sets in semigraphics 6 and full graphics
GM0-GM2	30, 29, 27	Graphic mode select; select one of eight graphic modes.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Rating	Value
Supply Voltage (V_{CC})	-0.3 to +7.0V
Input Voltage any Pin	-0.3 to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C
Power Dissipation	TBD

FORMAT OF THE TELEVISION SCREEN



*One on each non-interlaced line

DC (STATIC) CHARACTERISTICS – (V_{CC} = 5.0 V ±5%, V_{SS} = 0.0 V, T_A = 0°C to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ.	Max.	Unit
Input High Voltage Clk Other Inputs		V_{IH}	 V_{SS} + 2.4 V_{SS} + 2.0	 – –	 V_{CC} V_{CC}	Vdc
Input Low Voltage Clk Other Inputs		V_{IL}	 V_{SS} - 0.3 V_{SS} - 0.3	 – –	 V_{SS} + 0.4 V_{SS} + 0.8	Vdc
Input Leakage Current CLK, GM0-GM2, INV, $\overline{INT}$/EXT, $\overline{MS}$, V_{SS}, DD0-DD7, $\overline{A}/S$, $\overline{A}/G$		I_{in}	–	–	2.5	μAdc
Three-State (Off State) Input Current DA0-DA12		I_{LO}	–	–	10	μAdc
Output High Voltage (C_{Load} = 30 pF, I_{Load} = -100 μA)	$\overline{RP}$, $\overline{HS}$, $\overline{FS}$	V_{OH}	2.4	–	–	Vdc
Output High Voltage (C_{Load} = 55 pF, I_{Load} = -100 μA)	DA0-DA12	V_{OH}	2.4	–	–	Vdc
Output Load Voltage (C_{Load} = 30 pF, I_{Load} = 1.6 mA)	$\overline{RP}$, $\overline{HS}$, $\overline{FS}$	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output Low Voltage (C_{Load} = 55 pF, I_{Load} = 1.6 mA)	DA0-DA12	V_{OL}	–		V_{SS} + 0.4	Vdc
Output High Current (Sourcing) (V_{OH} = 2.4 V)	All Outputs (except φA, φB, Y, & CHB)	I_{OH}	-100	-		μAdc
Output Low Current (Sinking) (V_{OL} = 0.4 Vdc)	All Outputs (except φA, φB, Y, & CHB)	I_{OL}	1.6	–	–	mAdc
Input Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	All Inputs	C_{in}	–	–	7.5	pF
Chroma Bias Voltage (C_{Load} = 20 pF, R Load = 200 k ohm, V_{CC} = 4.75 – 5.25 V)		V_R	–	0.3 V_{CC}	–	Vdc

DC (STATIC) CHARACTERISTICS — (V_{CC} = 5.0 V ± 5%, V_{SS} = 0.0 V, T_A = 0°C to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ.	Max.	Unit
Chroma φA Voltage Figure 2	$V_{C\phi A}$				Vdc
(C_{Load} = 20 pF, R Load = 200 k ohm)	V_{HI}	–	V_R + 0.1 V_{CC}	–	
	V_0	–	V_R	–	
	V_{LO}		V_R – 0.1 V_{CC}	–	
Chroma φB Voltage	$V_{C\phi B}$				Vdc
(C_{Load} = 20 pF, R Load = 200 k ohm)			V_R + 0.1 V_{CC}	–	
V_0		–	V_R	–	
V_{burst}		–	V_R – 0.05 V_{CC}	–	
V_{LO}		–	V_R – 0.1 V_{CC}	–	
Luminance Y Voltage Figure 2	V_Y				Vdc
(C_{Load} = 20 pF, R_{Load} = 200 k ohm)	V_S	–	0.2 V_{CC}	–	
	V_{BLANK}	–	0.75 V_S	–	
	V_{BLACK}	–	0.7 V_S	–	
Voltage White Low Figure 2	V_{WL}	–	0.62 V_S	–	Vdc
(Voltage White Medium)	V_{WM}	–	0.5 V_S	–	
(Voltage White High)	V_{WH}	–	0.38 V_S	–	

AC (Dynamic) CHARACTERISTICS — V_{CC} = 5.0 V ± 5%, T_A = 0°C to 70°C

Characteristic	Symbol	Min	Typ.	Max.	Unit
Clk Frequency	f	3.579535	3.579545	3.579555	MHz
Clk Duty Cycle	Clk_{dc}	45%	50%	55%	
Chroma Phase Delay Figure 3C					ns
(measured with respect to "Y" output)					
φA	t_{YA}		200	–	
φB	t_{YB}		200	–	
Luminance Rise Time Figure 3D	t_{ry}	–	60	–	ns
Luminance Fall Time	t_{fy}	–	50	–	
Chroma Rise and Fall Times Figure 3D					ns
(φA Rise Time)	$t_rC\phi A$	–	60	–	
(φA Fall Time)	$t_fC\phi A$	–	60	–	
(φB Rise Time)	$t_rC\phi B$	–	60	–	
(φB Fall Time)	$t_fC\phi B$	–	60	–	
$\overline{\text{Field Sync}}$ ($\overline{\text{FS}}$) Figure 3A	t_{WFS}	–	2.03	–	ms
(Pulse Width)					
$\overline{\text{Row Preset}}$ ($\overline{\text{RP}}$) Figure 3B					
(Pulse Width)	t_{WRP}	–	0.98	–	μs
(Delay From $\overline{\text{HS}}$)	t_{HSRP}	–	0.98	–	μs
$\overline{\text{Horizontal Sync}}$ ($\overline{\text{HS}}$) Figure 3B	t_{WHS}	–	4.9	–	μs

FIGURE 2 – VIDEO AND CHROMINANCE RELATIONSHIPS OUTPUT WAVEFORM

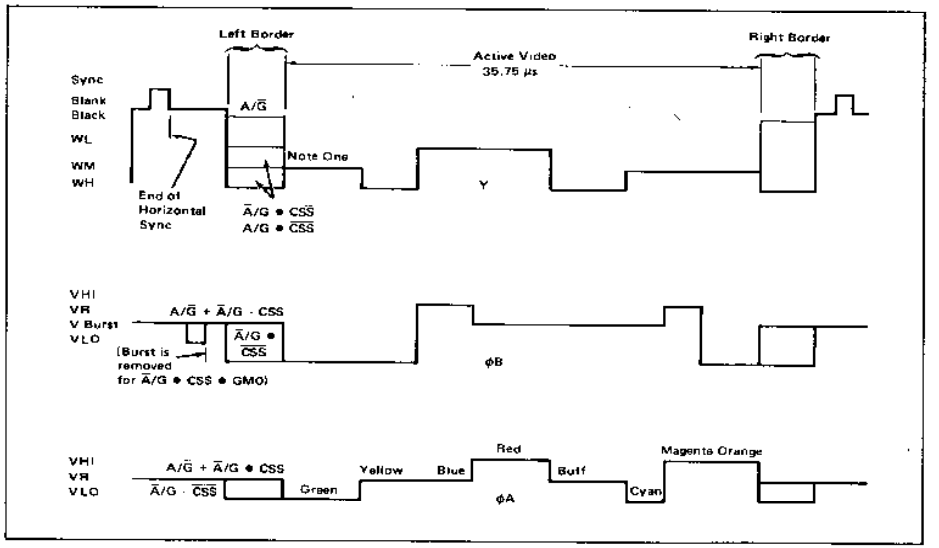
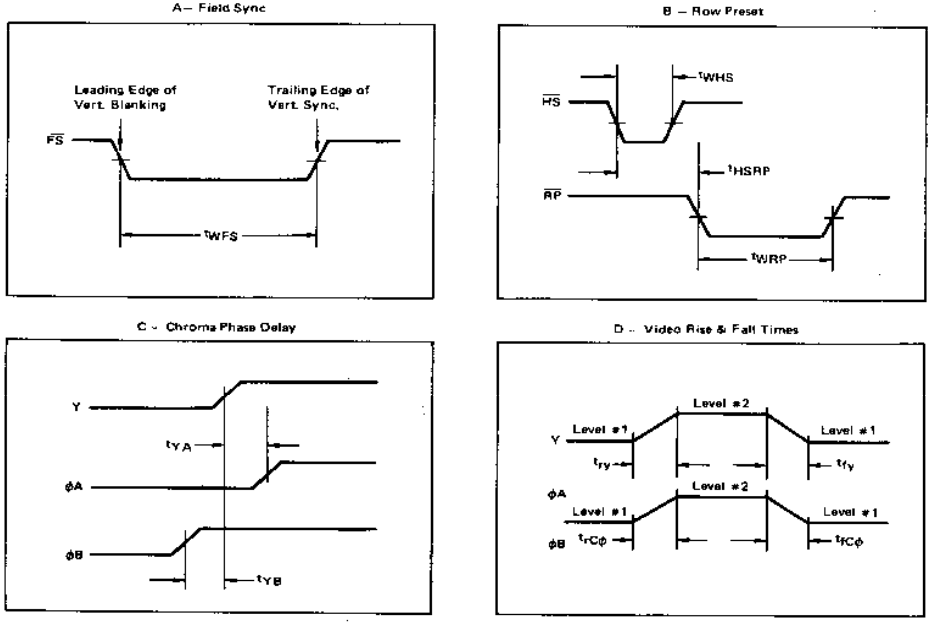


FIGURE 3 – TIMING DIAGRAMS



VDG SIGNAL DESCRIPTION

Address Output Lines (DA0-DA12) – Thirteen address lines are used by the VDG to scan the display memory. The starting address of the display memory is located at the upper left corner of the display screen. As the television sweeps from the left to right and top to bottom, the VDG increments the RAM display address. These lines are TTL compatible and may be forced into a high impedance state whenever the $\overline{MS}$ pin goes low.

Data Inputs (DD0-DD7) – Eight TTL compatible data lines are used to input data from RAM to be processed by the VDG. The data is interpreted and transformed into luminance Y (Pin 28) and color outputs ϕA and ϕB (Pin 11 and Pin 10).

Power Inputs – V_{CC} requires +5 volts. V_{SS} requires zero volts and is normally ground. The tolerance and current requirements of the VDG are specified in the Electrical Characteristics.

Video Outputs (ϕA, ϕB, Y, CHB) – These four analog outputs are used to transfer luminance and color information to a standard NTSC color television receiver, either via the MC1372 RF modulator or directly into Y, ϕA, ϕB television video inputs.

LUMINANCE (Y) – This six level analog output contains composite sync., blanking and four levels of video luminance.

ϕA – This three level analog output is used in combination with ϕB and Y outputs to specify one of eight colors.

ϕB – This four level analog output is used in combination with ϕA and Y outputs to specify one of eight colors. Additionally, one analog level is used to specify the time of the color burst reference signal.

CHROMA BIAS (CHB) – This pin is an analog output and provides a D.C. reference corresponding to the quiescent value of ϕA and ϕB. CHB is used to guarantee good thermal tracking and minimize the variation between the parts.

Synchronizing Inputs ($\overline{MS}$, CLK)

Three-State Control – ($\overline{MS}$) is a TTL compatible input which, when low, forces the VDG address lines into a high impedance state. This may be done to allow other devices (such as an MPU) to address the display memory (RAM).

Clock (CLK) – The VDG clock input (CLK) requires a 3.579545 MHz (standard) TV crystal frequency square wave. The duty cycle of this clock must be between 45 and 55 percent since it controls the width of alternate dots on the television screen. The MC1372 RF modulator may be used to supply the 3.579545 MHz clock and has provisions for a duty cycle adjustment.

Synchronizing Outputs ($\overline{FS}$, $\overline{HS}$, $\overline{RP}$) – Three TTL compatible outputs provide circuits, exterior to the VDG, with timing references to the following internal VDG states:

FIELD SYNC – ($\overline{FS}$) – The high to low transition of the $\overline{FS}$ output coincides with the end of active display area. During this time interval an MPU may have total access to the display RAM without causing undesired flicker on the screen. The Low to High transition of $\overline{FS}$ coincides with the trailing edge of the vertical synchronization pulse.

HORIZONTAL SYNC – ($\overline{HS}$) – The $\overline{HS}$ pulse is in coincidents with the horizontal synchronization pulse furnished to the television receiver by the VDG. The high to low transition of the $\overline{HS}$ output coincides with the leading edge of the horizontal synchronization pulse.

ROW PRESET – ($\overline{RP}$) – If desired, an external character generator ROM may be used with the VDG. However, an external four bit counter must be added to supply row selection. The counter is clocked by the $\overline{HS}$ signal and cleared by the $\overline{RP}$ signal.

Mode Control Lines (Input) ($\overline{A}$/G, $\overline{A}$/S, $\overline{INT}$/EXT, GM0, GM1, GM2, CSS, INV) – Eight TTL compatible inputs are used to control the operating mode of the VDG. $\overline{A}$/S, $\overline{INT}$/EXT, CSS and INV may be changed on a character by character basis. The CSS pin is used to select between two possible alphanumeric colors; when the VDG is in the alphanumeric mode and between two color sets when the VDG is in the semigraphics 6 and full Graphic mode. Table 1 illustrates the various modes that can be obtained using the mode control lines.

DISPLAY MODES

The VDG is capable of generating 12 distinct display modes (refer to Table 1). The color set selection and invert pins will allow variations on certain modes. The VDG will display two alphanumeric modes with two compatible semigraphic modes or display one of eight full graphic modes. A detailed description of the various modes of operation follows. A summary of major modes can be found in Table 2.

ALPHANUMERIC DISPLAY MODES – All alphanumeric modes occupy an 8 x 12 dot character matrix box and there are 32 x 16 character boxes per TV frame. Each horizontal dot (dot-clock) corresponds to one-half the period duration of the 3.58 MHz clock and each vertical dot is one scan line. One of two colors for the lighted dots may be selected by the color set select pin. An internal ROM will generate 64 ASCII display characters in a standard 5 x 7 box. Six bits of the eight-bit data word are used for the ASCII character generator and the two bits not used can be used to implement inverse video or color switching on a character by character basis. A 512 word display memory is required for this class of display.

The ALPHA SEMIGraphics-4 mode translates bits zero through three into a 4 x 6 dot element in the standard 8 x 12 dot box. Three data bits may be used to select one of eight colors for the entire character box. The extra bit is available to implement mode switching on the fly. A 512 word display memory is required. A density of 64 x 32 elements is available in the display area. The element area is four dot-clocks wide by six lines high.

The ALPHA SEMIGraphic-6 mode maps six 4 x 4 dot elements into the standard 8 x 12 dot alphanumeric box, a screen density of 64 x 48 elements is available. Six bits are used to generate this map and two data bits may be used to select one of four colors in the display box. The element area is four dot-clocks wide by four lines high.

FULL GRAPHIC MODE – There are eight full graphic modes available from the VDG. These modes require 1K to 6K bytes of memory. The eight full-graphic modes include an outside color border in one of two colors depending upon the color set select pin (CSS). The CSS pin selects one of two sets of four colors in the four color graphic modes.

The 64 x 64 Color Graphics Mode – The 64 x 64 color graphics mode generates a display matrix of 64 elements wide by 64 elements high. Each element may be one of four colors. A 1K x 8 display memory is required. Each pictel equals four dot-clocks by three scan lines.

The 128 x 64 Graphics Mode – The 128 x 64 graphics mode generates a matrix 128 elements wide by 64 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors, selected by using the color set select pin. A 1K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 64 Color Graphics Mode – The 128 x 64 color graphics mode generates a display matrix 128 elements wide by 64 elements high. Each element may be one of four colors. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 96 Graphics Mode – The 128 x 96 graphics mode generates a display matrix 128 elements wide by 96 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors selected by using the color select pin. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 96 Color Graphics Mode – The 128 x 96 color graphics mode generates a display 128 elements wide by 96 elements high. Each element may be one of four colors. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 192 Graphics Mode – The 128 x 192 graphics mode generates a display matrix 128 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON elements may be one of two colors selected with color set select pin. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by one scan line.

The 128 x 192 Color Graphics Mode – The 128 x 192 color graphics mode generates a display 128 elements wide by 192 elements high. Each element may be one of four colors. A 6K x 8 display memory is required. A detailed description of the VDG modes is given in Table 3. Each pictel equals two dot-clocks by one scan line.

The 256 x 192 Graphics Mode – The 256 x 192 graphics mode generates a display 256 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON element may be one of two colors selected with the color set select pin. A 6K x 8 display memory is required. Each pictel equals one dot-clock by one scan line.

TABLE 1 – TABLE OF MODE CONTROL LINES (INPUTS)

Ā/G	Ā/S	INT/EXT	INV	GM2	GM1	GM0	ALPHA/GRAPHIC MODE SELECT
0	0	0	0	X	X	X	Internal Alphanumerics
0	0	0	1	X	X	X	Internal Alphanumerics Inverted
0	0	1	0	X	X	X	External Alphanumerics
0	0	1	1	X	X	X	External Alphanumerics Inverted
0	1	0	X	X	X	X	Semigraphics - 4
0	1	1	X	X	X	X	Semigraphics - 6
1	X	X	X	0	0	0	64 x 64 Color Graphics
1	X	X	X	0	0	1	128 x 64 Graphics
1	X	X	X	0	1	0	128 x 64 Color Graphics
1	X	X	X	0	1	1	128 x 96 Graphics
1	X	X	X	1	0	0	128 x 96 Color Graphics
1	X	X	X	1	0	1	128 x 192 Graphics
1	X	X	X	1	1	0	128 x 192 Color Graphics
1	X	X	X	1	1	1	256 x 192 Graphics

TABLE 2 – SUMMARY OF MAJOR MODES

MAJOR MODE ONE
TABLE OF ALPHA MINOR MODES

Title	Memory	Colors	Display Elements
Alphanumeric (Internal)	512 x 8	2	
Alphanumeric (External)	512 x 8	2	
Alpha Semig-4	512 x 8	8	Box / Element
Alpha Semig-6	512 x 8	4	Box / Element

MAJOR MODE TWO
TABLE OF MINOR GRAPHICS MODES

Title	Memory	Colors	Comments
64 x 64 Color Graphic	1K x 8	4	Matrix 64 x 64 Elements
128 x 64 Graphics*	1K x 8	2	Matrix 128 elements wide by 64 elements high
128 x 64 Color Graphic	2K x 8	4	
128 x 96 Graphics*	1.5K x 8	2	Matrix 128 elements wide by 96 elements high
128 x 96 Color Graphic	3K x 8	4	
128 x 192 Graphics*	3K x 8	2	Matrix 128 elements wide by 192 elements high
128 x 192 Color Graphic	6K x 8	4	
256 x 192 Graphics*	6K x 8	2	Matrix 256 elements wide by 192 elements high

*Graphics mode turns on or off each element. The color may be one of two.

TABLE 3 – DETAILED DESCRIPTION OF VDG MODES

$\overline{MS}$	Ā/G	Ā/S	INT/EXT	GM2	GM1	GM0	CSS	INV	Character Color	Background	Border	Display Mode	Detail	VDG Data Bus	Comments
1	0	0	0	X	X	X	0 / 1	0 / 1	Green / Black (CSS 0); Orange / Black (CSS 1)	Black / Green (CSS 0); Black / Orange (CSS 1)	Black / Black	32 Characters across, 16 Characters down	5 dots × 7 dots character in 8 dots × 12 dots	ASCII code	The ALPHANUMERIC INTERNAL mode uses an internal character generator which contains the following five dot by seven dot characters: @ABCDEFGHIJKLMNOPQRSTUVWXYZ[\]↑← !"#$%&'()*+,-./0123456789:;<=>? The six bit ASCII code leaves two bits free and these may be externally connected to the mode pins (Ā/G, Ā/S, INT/EXT, GM2, GM1, GM0, CSS or INV).
1	0	0	1	X	X	X	0 / 1	0 / 1	Green / Black (CSS 0); Orange / Black (CSS 1)	Black / Green (CSS 0); Black / Orange (CSS 1)	Black / Black	32 Characters across, 16 Characters down		one row of custom characters	The ALPHANUMERIC EXTERNAL mode uses an external character generator as well as a row counter. Thus, custom character fonts or graphic symbol sets with up to 256 different eight dot x 12 dot "characters" may be displayed.
1	0	1	0	X	X	X	X	X	L: 0 1 1 1 1 1 1 1 1; C2: X 0 0 0 0 1 1 1 1; C1: X 0 0 1 1 0 0 1 1; C0: X 0 1 0 1 0 1 0 1	Color: Black, Green, Yellow, Blue, Red, Buff, Cyan, Magenta, Orange	Black	64 Display elements across, 32 Display elements down	L_3 L_2 / L_1 L_0 (one element)	C_2 C_1 C_0 L_3 L_2 L_1 L_0	The SEMIGRAPHICS FOUR mode uses an internal "coarse graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by three bits.
1	0	1	1	X	X	X	0 / 1	X	L: 0 1 1 1 1 0 1 1 1 1; C1: X 0 0 1 1 X 0 0 1 1; C0: X 0 1 0 1 X 0 1 0 1	Color: Black, Green, Yellow, Blue, Red, Black, Buff, Cyan, Magenta, Orange	Black	64 Display elements across, 48 Display elements down	L_5 L_4 / L_3 L_2 / L_1 L_0	C_1 C_0 L_5 L_4 L_3 L_2 L_1 L_0	The SEMIGRAPHIC SIX mode is similar to the SEMIGRAPHIC FOUR mode with the following differences. The eight dot by twelve dot rectangle is divided into six equal parts. Color is determined by the two remaining bits.
1	1	X	X	0	0	0	0 / 1	X	C1: 0 0 1 1 0 0 1 1; C0: 0 1 0 1 0 1 0 1	Color: Green, Yellow, Blue, Red, Buff, Cyan, Magenta, Orange	Green / Buff	64 Display elements across, 64 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS ONE C mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.
1	1	X	X	0	0	1	0 / 1	X	L: 0 1 0 1	Color: Black, Green, Black, Buff	Green / Buff	128 Display elements across, 64 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS ONE R mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element.
1	1	X	X	0	1	0	0 / 1	X	Same color as Graphics one C		Green / Buff	128 Display elements across, 64 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS TWO C mode uses a maximum of 2048 bytes of display RAM in which one pair of bits specifies one picture element.
1	1	X	X	0	1	1	0 / 1	X	Same color as Graphics one R		Green / Buff	128 Display elements across, 96 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS TWO R mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.
1	1	X	X	1	0	0	0 / 1	X	Same color as Graphics one C		Green / Buff	128 Display elements across, 96 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS THREE C mode uses a maximum of 3072 bytes of display RAM in which one pair of bytes specifies one picture element.
1	1	X	X	1	0	1	0 / 1	X	Same color as Graphics one R		Green / Buff	128 Display elements across, 192 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS THREE R mode uses a maximum of 3072 bytes of display RAM in which one bit specifies one picture element.
1	1	X	X	1	1	0	0 / 1	X	Same color as Graphics one C		Green / Buff	128 Display elements across, 192 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS SIX C mode uses a maximum of 6144 bytes of display RAM in which one pair of bits specifies one picture element.
1	1	X	X	1	1	1	0 / 1	X	Same color as Graphics one R		Green / Buff	256 Display elements across, 192 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS SIX R mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element.

TABLE 3 – DETAILED DESCRIPTION OF VDG MODES

VDG PINS									COLOR			TV SCREEN		VDG DATA BUS	COMMENTS
~~A/G~~	A/G	A/S	INT/EXT	GM2	GM1	GM0	CSS	INV	Character Color	Background	Border	Display Mode	Detail		
1	0	0	0	x	x	x	0	0	Green	Black	Black	32 Characters across 16 Characters down	8 dots, 12 dots, 7, 5	extra, ASCII code	The ALPHANUMERIC INTERNAL mode uses an internal character generator which contains the following five dot by seven dot characters @ABCDEFGHIJ KLMNOPQRSTUVWXYZ[\] ↑ ← SP !"#$%&'()*+,-./0123456789 :;< =>?. The six bit ASCII code leaves two bits free and these may be externally connected to the mode pins (A/G, A/S, INT/EXT, GM2, GM1, GM0, CSS or INV).
								1	Black	Green					
							1	0	Orange	Black					
								1	Black	Orange					
1	0	0	1	x	x	x	0	0	Green	Black	Black	32 Characters across 16 Characters down		one row of custom characters	The ALPHANUMERIC EXTERNAL mode uses an external character generator as well as a row counter. Thus, custom character fonts are graphic symbol sets with up to 256 different eight dot x 12 dot "characters" may be displayed.
								1	Black	Green					
							1	0	Orange	Black					
								1	Black	Orange					
1	0	1	0	x	x	x	x	x	Lx C2 C1 C0 Color 0 x x x Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Blue 1 0 1 1 Red 1 1 0 0 Buff 1 1 0 1 Cyan 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements across 32 Display elements down	L_3 L_2 / L_1 L_0 one element	C_2 C_1 C_0 L_3 L_2 L_1 L_0	The SEMIGRAPHICS FOUR mode uses an internal "course graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by three bits.
1	0	1	1	x	x	x	0	x	Lx C1 C0 Color 0 x x Black 1 0 0 Green 1 0 1 Yellow 1 1 0 Blue 1 1 1 Red 0 x x Black 1 0 0 Buff 1 0 1 Cyan 1 1 0 Magenta 1 1 1 Orange		Black	64 Display elements across 48 Display elements down	L_5 L_4 / L_3 L_2 / L_1 L_0	C_1 C_0 L_5 L_4 L_3 L_2 L_1 L_0	The SEMIGRAPHIC SIX mode is similar to the SEMIGRAPHIC FOUR mode with the following differences. The eight dot by twelve dot rectangle is divided into six equal parts. Color is determined by the two remaining bits.
1	1	x	x	0	0	0	0	x	C1 C0 Color 0 0 Green 0 1 Yellow 1 0 Blue 1 1 Red 0 0 Buff 0 1 Cyan 1 0 Magenta 1 1 Orange		Green / Buff	64 Display elements across 64 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS ONE C mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.
1	1	x	x	0	0	1	0	x	Lx Color 0 Black 1 Green		Green / Buff	128 Display elements across 64 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS ONE R mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element.
							1	x	0 Black 1 Buff						
1	1	x	x	0	1	0	0	x	Same color as Graphics one C		Green / Buff	128 Display elements across 64 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS TWO C mode uses a maximum of 2048 bytes of display RAM in which one pair of bits specifies one picture element.
1	1	x	x	0	1	1	0	x	Same color as Graphics one R		Green / Buff	128 Display elements across 96 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS TWO R mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.
							1	x							
1	1	x	x	1	0	0	0	x	Same color as Graphics one C		Green / Buff	128 Display elements across 96 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS THREE C mode uses a maximum of 3072 bytes of display RAM in which one pair of bytes specifies one picture element.
							1	x							
1	1	x	x	1	0	1	0	x	Same color as Graphics one R		Green / Buff	128 Display elements across 192 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS THREE R mode uses a maximum of 3072 bytes of display RAM in which one bit specifies one picture element.
							1	x							
1	1	x	x	1	1	0	0	x	Same color as Graphics one C		Green / Buff	128 Display elements across 192 Display elements down	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS SIX C mode uses a maximum of 6144 bytes of display RAM in which one pair of bits specifies one picture element.
							1	x							
1	1	x	x	1	1	1	0	x	Same color as Graphics one R		Green / Buff	256 Display elements across 192 Display elements down	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS SIX R mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element.
							1	x							